IT IS CLAIMED:

1. In a memory system including a plurality of units of erasable and re-programmable non-volatile memory cells having contiguous physical addresses organized into zones with address boundaries therebetween and wherein a distinct range of logical addresses are mapped into each of the zones, a method of operation that comprises:

reassigning the boundary addresses to delete at least one unit from each of the zones and to add said at least one unit to an adjacent zone without changing the number of units in the individual zones,

thereafter accessing the zones for programming data to or reading data from the reassigned memory cell units therein according to logical addresses of the data, and

repetitively reassigning the boundary addresses and accessing the zones at least until the memory cell units have all been moved from their zones to adjacent zones, thereby to spread out usage of the units accessed through the logical addresses.

2. The method of claim 1, wherein reassigning the boundary addresses includes deleting a number of units from each of the zones less than ten percent of the units within the zone and adding said number of units to an adjacent zone.

3. The method of claim 1, wherein the zones are formed with portions of their memory cell units in an individual plurality of memory planes, and wherein reassigning the boundary addresses includes deleting at least one unit from each portion of the zones in each of the memory planes and adding said at least one unit to an adjacent portion of another zone within the same plane.

4. The method of claim 1, wherein the memory cell units individually include a plurality of simultaneously erasable memory cells.

5. The method of claim 4, wherein the memory cell units individually include a plurality of pages that are individually programmable with data.

6. The method of claim 1, wherein reassigning the boundary addresses includes copying any data stored in said at least one unit from each of the zones into the added unit of the adjacent zone.

7. A method of operating a system of erasable and re-programmable non-volatile memory cells that are physically organized into units of a minimum number of memory cells that are simultaneously erasable, comprising:

directing host access requests to program or read data within one of three or more non-overlapping ranges of logical memory addresses into a unique one of a corresponding number of logical groups of memory cell erase units,

mapping access requests from the logical groups into distinct physical groups of a plurality of erase units, and

between data programming or reading operations caused by host access requests, repetitively re-mapping the logical groups into the physical groups by removing a portion of the individual physical groups including at least one erase unit at a time and adding the removed erase units to adjacent ones of the physical groups in a manner that maintains a uniform number of erase units in the individual physical groups, whereby usage of the erase units over the system is leveled out over time.

8. A method of operating an array of flash memory cells organized into a plurality of blocks of a minimum number of simultaneously erasable memory cells within a plurality of planes, comprising:

defining a plurality of zones to individually include a portion of the plurality of blocks from each of a plurality of planes,

mapping a different portion of a range of logical addresses to each of the zones, and

repetitively re-defining the individual zones by removing at least one block therefrom in each plane and adding the removed blocks to others of the zones in their same planes in a manner to maintain the plurality of zones with the specified plurality of blocks in each of the plurality of planes, whereby usage of the blocks at various of the ranges of logical addresses is spread out in time over the array.

9. In a memory system including a plurality of zones individually including a plurality of units of re-programmable non-volatile memory cells that are erasable together, wherein a distinct range of logical addresses received by the memory system are mapped into the individual zones, a method of operation that comprises:

receiving a logical address within the distinct logical address range of one of the zones, and

converting the received logical address into a physical address of at least one of the plurality of memory cell erase units within said one zone that tends to even out a number of usage cycles of erasing and re-programming the erase units within said one zone.

10. The method of claim 9, wherein converting the logical address into the physical address includes reference to a table of corresponding logical and physical addresses, and which additionally comprises changing the correspondence between logical and physical erase unit addresses in order to tend to even out the frequency of use of the erase units within said one zone.

11. The method of claim 10, wherein changing the correspondence between logical and physical erase unit addresses includes swapping physical addresses of the erase units within said one zone that have a highest and a lowest accumulated number of usage cycles.

12. The method of claim 10, wherein the memory cells have a target endurance limit of a maximum number of usage cycles that the memory cells are to experience, and wherein changing the correspondence between logical and physical erase unit addresses occurs prior to the number of usage cycles of an erase unit whose corresponding address is changed reaching said target maximum number.

13. In a memory system including a plurality of zones individually including a plurality of units of re-programmable non-volatile memory cells that are erasable together, wherein a distinct range of logical addresses received by the memory system are mapped into the individual zones, a method of operation that comprises:

exchanging data stored in a first of the plurality of zones with data stored in a second of the plurality of zones, and

thereafter converting addresses accessing the memory system within one of the first and second zones to addresses accessing the other of the first and second zones.

14. The method of claim 13, wherein exchanging data includes:

moving data from a first erase unit in the second zone having a physical address adjacent a border of physical addresses of the second zone into a second erase unit in the second zone that is erased, and

moving data from an erase unit of the first zone having a physical address adjacent a border of physical addresses of the first zone into said first unit.

15. A method of operating a system of erasable and re-programmable non-volatile memory cells organized into a plurality of physical blocks of a minimum number of memory cells that are simultaneously erasable and wherein incoming data are programmed into those of the plurality of physical blocks maintained as an erased block pool, comprising:

identifying at least one of the plurality of physical blocks at a time other than those in the erased block pool for a wear leveling exchange by cycling through addresses of the plurality of physical blocks in a predefined order, and

exchanging the identified at least one of the plurality of physical blocks with a corresponding number of at least one of the plurality of physical blocks within the erased block pool.

16. The method of claim 15, wherein exchanging the identified blocks includes copying data from the identified at least one of the plurality of physical blocks into said corresponding number of at least one of the physical blocks within the erased block pool, and changing mapping of at least one logical block address from said at least one of the plurality of physical blocks to said corresponding number of at least one of the physical blocks within the erased block pool.

17. The method of claim 16, additionally comprising, after copying the data, of erasing the identified at least one of the plurality of physical blocks and placing the erased at least one block into the erase pool.

18. The method of claim 15, wherein identifying at least one of the plurality of physical blocks for a wear leveling exchange is accomplished without reference to a number of erase cycles experienced by the individual physical blocks.

19. The method of claim 15, wherein identifying at least one of the plurality of physical blocks at a time includes doing so at intervals of a predetermined number of the plurality of physical blocks within the erased block pool being programmed with data.

20. A method of operating a system of erasable and re-programmable non-volatile memory cells organized into a plurality of physical blocks of a minimum number of memory cells that are simultaneously erasable, comprising:

mapping a range of logical block addresses into addresses of a proportion of the plurality of physical blocks that leaves an additional number of physical blocks providing an erased block pool,

in response to requests to store data in at least one of the range of logical block addresses, converting said at least one logical block address into an address of at least one physical block residing in the erased block pool and then writing the data into said at least one physical block of the erased block pool,

identifying one of the plurality of physical blocks for a wear leveling exchange,

after a given number of memory programming operations, exchanging the identified one of the plurality of physical blocks with one of the number of physical blocks residing in the erased block pool, and

repeating identifying and exchanging with others of the plurality of physical blocks in a predefined order.

21. The method of claim 20, wherein identifying physical blocks includes determining whether the identified physical block is within the erase block pool or subject to a pending programming operation, in either case the identified physical block is not exchanged.

22. The method of claim 20, wherein exchanging the identified blocks includes copying data from the identified one of the plurality of physical blocks into said corresponding number of physical blocks within the erased block pool, and changing mapping of at least one logical block

address from said at least one of the plurality of physical blocks to said corresponding number of one or more physical blocks within the erased block pool.

23. The method of claim 22, additionally comprising, after copying the data, of erasing the identified one of the plurality of physical blocks and placing the erased at least one block into the erase pool.

24. A method of managing groups of erasable and electrically programmable memory cells, comprising:

upon programming data into various groups of cells, associating and storing one of a plurality of indications for the individual programmed groups of cells that is selected by incrementing the indication after a predefined number of instances of programming have occurred, the associated and stored indications being repetitively incremented through the plurality of indications in a predefined order, wherein the stored indications provide relative times of programming of the corresponding groups of cells, and

performing an operation on the groups of memory cells according to their relative numbers assigned.

25. The method of claim 24, wherein associating and storing the indications include associating a first of a plurality of indications to the groups of cells being programmed until said first indication has been assigned to a predefined number of programmed groups of cells, thereafter assigning a second of the plurality of indications to the groups being programmed until the second of the plurality of indications has been assigned to a predefined number of groups of cells, and thereafter associating a third of a plurality of indications to the groups being programmed until the third of the plurality of indications has been associated with a predefined number of groups of cells.

26. The method of claim 24, wherein the plurality of indications include a plurality of sequential numbers.

27. The method of claim 24, wherein the operation performed on the groups of memory cells includes selecting those of the groups of cells for programming according to the relative

indications applied to the groups in a manner that tend to even out a number of cycles of programming experienced by the groups.